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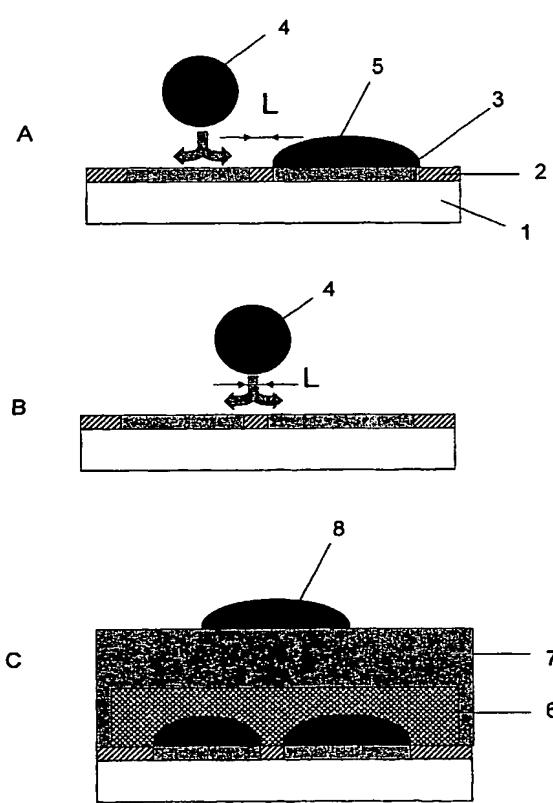
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(54) Title: SEMICONDUCTING ISLAND AS ACTIVE LAYER IN FET



(57) Abstract: A method for forming an electronic device including at least one electrically conductive and one semiconductive material deposited from solution, the method comprising: forming on the substrate a confinement structure consisting of a least a first zone and a second zone, depositing the electrically conductive material on the substrate, wherein the electrically conductive material is absent from both the first and second zone, and subsequently depositing the electrically semiconductive material from solution, wherein the semiconductive material is absent from the first zone, but not from the second zone.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 H01L51/40 H01L51/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	WO 01/46987 A (PLASTIC LOGIC LTD ; SIRRINGHAUS HENNING (GB); KAWASE TAKEO (GB); FRIEN) 28 June 2001 (2001-06-28)	1,2,5-7, 10, 12-19, 22, 33-35, 37,38, 48,50,51
Y	page 6, line 17 - page 7, line 3 page 42, line 17 - line 21; figure 21a	45-47
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Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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